Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-45 (cancelled)

46. (currently amended) A field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a trench extending a predetermined depth into the semiconductor substrate;

a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the semiconductor substrate to form a well junction at a first depth;

a doped source region having dopants of the first conductivity type and extending into the semiconductor substrate to form a source junction at a second depth; and

a doped heavy body region having dopants of the second conductivity type and extending into the doped well to form a heavy body junction at a depth that is deeper than the source junction and shallower than the depth of the trench,

wherein the heavy body region forms an abrupt junction in the doped well ~~to direct breakdown current away from the trench~~.

47. (previously presented) The field effect transistor of claim 46 wherein a location of the abrupt junction relative to the well junction at the second depth is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the trench in the semiconductor.

48. (previously presented) The field effect transistor of claim 46 wherein the doped well has a substantially flat bottom.

49. (previously presented) The field effect transistor of claim 46 wherein the trench has rounded top corners.

50. (previously presented) The field effect transistor of claim 46 wherein the trench has rounded bottom corners.

51. (previously presented) The field effect transistor of claim 46 wherein the trench has rounded top and bottom corners.

52. (previously presented) The field effect transistor of claim 46 wherein the heavy body comprises a heavily doped region formed by implanting dopants of the second conductivity type at an approximate location of the abrupt junction.

53. (previously presented) The field effect transistor of claim 46 wherein the trench is lined with a dielectric material and substantially filled with conductive material, wherein the conductive material substantially filling the trench is recessed relative to the surface of the substrate.

54. (previously presented) The field effect transistor of claim 46 wherein the substrate comprises a first highly doped region and a second doped region disposed above said first highly doped region, the second doped region having a lower doping concentration relative to the first highly doped region.

55. (previously presented) The field effect transistor of claim 54 further comprising a termination structure surrounding the transistor.

56. (previously presented) The field effect transistor of claim 55 wherein the termination structure comprises a doped region having dopants of the second conductivity type

extending into the second doped region of the substrate to form a PN junction between the termination doped region and the second doped region of the substrate.

57. (previously presented) The field effect transistor of claim 55 wherein the termination structure comprises a trench.

58. (previously presented) The field effect transistor of claim 55 wherein the termination structure comprises a plurality of concentric trenches surrounding the transistor.

59. (previously presented) The field effect transistor of claim 57 wherein the termination trench extends to substantially the same depth as the transistor trench.

60. (previously presented) The field effect transistor of claim 54 wherein the second doped region of the substrate has an initial thickness of less than 10μm.

61. (previously presented) The field effect transistor of claim 54 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is less than 3μm.

62. (previously presented) The field effect transistor of claim 54 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is approximately 1μm.

63. (previously presented) The field effect transistor of claim 46 wherein the depth of the doped well ranges from approximately 1μm to 3μm.

64. (previously presented) The field effect transistor of claim 46 wherein the depth of the doped heavy body ranges from approximately 0.4μm to 1.5μm.

65. (previously presented) The field effect transistor of claim 46 wherein a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately 0.5μm to 1.5μm.

66. (previously presented) The field effect transistor of claim 46 wherein a distance between a bottom of the doped heavy body to the doped well junction is less than approximately 0.5μm.

67. (currently amended) A field effect transistor comprising:

a semiconductor substrate having dopants of a first conductivity type;

a plurality of gate-forming trenches arranged substantially parallel to each other, each trench extending to a first depth into said substrate, the space between adjacent trenches defining a contact area;

a doped well having dopants of a second conductivity type opposite to the first conductivity type and extending into the semiconductor substrate to form a well junction with the substrate;

a doped source region having dopants of the first conductivity type forming a source junction inside the doped well;

a heavy body having dopants of the second conductivity type and extending into the doped well to a second depth that is deeper than the source junction; and

heavy body contact regions defined at the surface of the semiconductor substrate along the length of the contact area,

wherein the heavy body forms an abrupt junction within the doped well ~~to direct breakdown current away from the trenches~~.

68. (previously presented) The field effect transistor of claim 67, wherein said doped well has a substantially flat bottom.

69. (previously presented) The field effect transistor of claim 67 wherein a location of the abrupt junction relative to the well junction at the second depth is adjusted so that, when voltage is applied to the transistor, a peak electric field is spaced away from the plurality of gate-forming trenches.

70. (previously presented) The field effect transistor of claim 67 wherein said doped well has a depth less than the first depth of the gate-forming trenches.

71. (previously presented) The field effect transistor of claim 67 wherein each said gate-forming trench has rounded top corners.

72. (previously presented) The field effect transistor of claim 67 wherein each said gate-forming trench has rounded bottom corners.

73. (previously presented) The field effect transistor of claim 67 wherein each said gate-forming trench has rounded top and bottom corners.

74. (previously presented) The field effect transistor of claim 67 further comprising a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a depth greater than the first depth of the plurality of gate-forming trenches.

75. (previously presented) The field effect transistor of claim 74 wherein the deep doped region forms a PN junction diode with the substrate.

76. (previously presented) The field effect transistor of claim 74 wherein the deep doped region forms a field termination structure surrounding the periphery of the plurality of gate-forming trenches.

77. (previously presented) The field effect transistor of claim 76 further comprising:

a layer of dielectric material formed over the deep doped region; and

a layer of conductive material formed on top of the layer of dielectric material.

78. (previously presented) The field effect transistor of claim 67 further comprising a field termination structure comprising a trench substantially surrounding the plurality of gate-forming trenches.

79. (previously presented) The field effect transistor of claim 78 wherein said field termination structure comprises a plurality of concentrically arranged trenches.

80. (previously presented) The field effect transistor of claim 67 wherein the heavy body forms a continuous doped region along substantially the entire length of said contact area.

81. (previously presented) The field effect transistor of claim 67 wherein said doped source region extends along the length of the trench.

82. (previously presented) The field effect transistor of claim 81 further comprising a source contact region defined at the surface of the semiconductor substrate and configured to contact the doped source region.

83. (previously presented) The field effect transistor of claim 81 further comprising a plurality of source contact regions disposed along the length of the contact area in an alternating fashion with the plurality of heavy body contact regions.

84. (previously presented) The field effect transistor of claim 67 wherein between a pair of adjacent trenches a plurality of doped source regions are positioned on opposite sides of

each trench, and wherein the heavy body is bounded by the pair of adjacent trenches and the doped source regions.

85. (previously presented) The field effect transistor of claim 67 wherein between a pair of adjacent trenches, the heavy body extends continuously parallel to the longitudinal axis of the trenches.

86. (previously presented) The field effect transistor of claim 67 further comprising:

a layer of dielectric material lining inside walls of each of said plurality of gate-forming trenches; and

a layer of conductive material substantially filling the gate-forming trenches.

87. (previously presented) The field effect transistor of claim 86 wherein the layer of conductive material comprises polysilicon.

88. (previously presented) The field effect transistor of claim 86 wherein the top surface of the layer of conductive material substantially filling the gate-forming trenches is recessed relative to the top surface of the semiconductor substrate.

89. (new) The field effect transistor of claim 67 wherein the substrate comprises a first highly doped region and a second doped region disposed above said first highly doped region, the second doped region having a lower doping concentration relative to the first highly doped region.

90. (previously presented) The field effect transistor of claim 89 wherein the second doped region of the substrate has an initial thickness of less than 10μm.

91. (previously presented) The field effect transistor of claim 89 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is less than 3μm.

92. (previously presented) The field effect transistor of claim 89 wherein the doped well extends into the second doped region of the substrate such that the resulting thickness of the second doped region of the substrate is approximately 1μm.

93. (previously presented) The field effect transistor of claim 67 wherein the depth of the doped well ranges from approximately 1μm to 3μm.

94. (previously presented) The field effect transistor of claim 67 wherein the depth of the doped heavy body ranges from approximately 0.4μm to 1.5μm.

95. (previously presented) The field effect transistor of claim 67 wherein a distance between a bottom of the doped heavy body to the doped well junction ranges from approximately 0.5μm to 1.5μm.

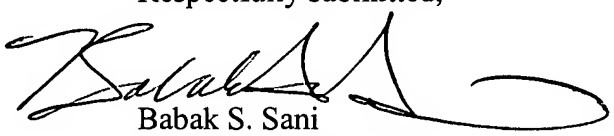
96. (previously presented) The field effect transistor of claim 67 wherein a distance between a bottom of the doped heavy body to the doped well junction is less than approximately 0.5μm.

CONCLUSION

Entrance of the foregoing amendments prior to examination of this application is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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